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Investigation on Dynamic Voltage Restorers With Two DC Links and Series Converters for Three-Phase Four-Wire Systems

Gregory A. A. Carlos*†, Cursino B. Jacobina† and Euzeli C. dos Santos Jr.‡
* DCIP - Federal Institute of Alagoas (IFAL) - Alagoas - Brazil
† DEE - Federal University of Campina Grande (UFCG) - Paraíba - Brazil
‡DECE - Purdue School of Engineering and Technology (IUPUI) - Indiana - USA

***Abstract*—This paper proposes three dynamic voltage restorer (DVR) topologies. Such configurations are able to compensate voltage sags/swells in three-phase four-wire (3P4W) systems under balanced and unbalanced conditions. The proposed systems use two independent dc links. Proposed configurations present advantages in terms of switch blocking voltages and consequently lower dc-link voltage rating. The complete control system, including the PWM technique, is developed and comparisons between the proposed configurations and a conventional one are performed. Simulation and experimental results are provided to validate the theoretical approach.**

***Index Terms*—Dynamic voltage restorer (DVR), open-end winding (OEW) transformer, three-phase four-wire system, multilevel inverter.**

NOMENCLATURE

j	Subscript associated for each system phase $j = 1, 2, 3$.
k	Subscript associated for each converter wire $k = 1, 2, 3, 4$.
q_{ak}, $\overline{q}_{ak}$	Homonymous binary variable and its complementary value for converter A.
q_{bk}, $\overline{q}_{bk}$	Homonymous binary variable and its complementary value for converter B.
v_{ak0a}	Pole voltages for converter A.
v_{bk0b}	Pole voltages for converter B.
v_{rk}	Resultant converter output voltages ($v_{rk} = v_{ak0a} - v_{bk0b}$).
v_{pj}	Phase voltages of injection transformers.
v^*_{xk}	References for auxiliary variables in the PWM strategy.
μ^*_{xk}	Parameters used to compute v^*_{xk}.
v^*_{r4}	Reference for fourth wire auxiliary variable in the PWM strategy.
μ^*_{r4}	Parameter used to compute v^*_{r4}.
v_{ca}, v^*_{ca}	Dc-link voltage for converter A and its reference.
v_{cb}, v^*_{cb}	Dc-link voltage for converter B and its reference.
v^*_{cab}	Average dc-link reference voltage.
$WTHD$	Weighted total harmonic distortion.
$IGBT$	Insulate gate bipolar transistor.
DSP	Digital signal processor.
f_s	Switching frequency.
f_o	Fundamental system frequency.
$4L$	Terminology used for conventional four-leg converter.
$2C$	Terminology used for conventional split-capacitor converter.
$3HB$	Terminology used for conventional three-H-bridge converter.
$2C2C$	Terminology used for proposed combined 2C-2C converter.
$4L2C$	Terminology used for proposed combined 4L-2C converter.
$4L4L$	Terminology used for proposed combined 4L-4L converter.
NPC	Terminology used for multilevel neutral-point-clamped converter.
$4LNPC$	Terminology used for four-leg NPC converter.
CHB	Terminology used for cascaded H-Bridge converter.
PLL	Phase-locked loop.
ESR	Equivalent series resistance.
P^{HO}_{loss}	Dc-link high frequency power losses.
C_f, C	Filtering capacitor and dc-link capacitor.

I. INTRODUCTION

Every year, the industry and commerce sector lose billions of dollars due to problems associated to power quality [1], [2]. Because of this fact, voltage sags have been reported as a major power-quality problem [3], [4]. In this way, dynamic voltage restorer (DVR) has been pointed out as the most attractive solution for this issue [5]–[10]. Such a customized power device is extremely suitable for protecting sensitive loads from voltage sags [10], [11]. The DVR is constituted by injection transformer, energy storage devices, passive filters (e.g., filtering capacitors) and PWM inverters, as observed in Fig. 1. This device is most applicable in distribution systems [6], [10] where voltage sags occur most commonly.

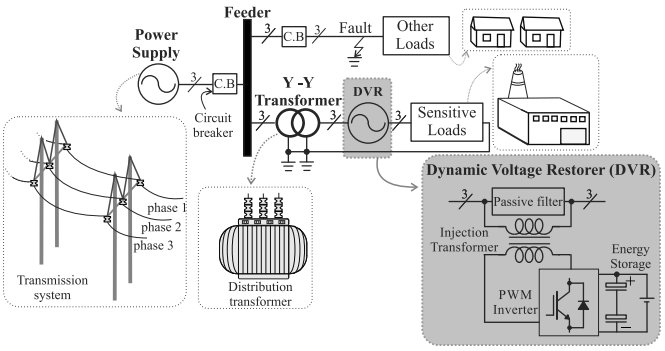

Fig. 1. Typical DVR location in a 3P4W power distribution system.

There are two types of power distribution systems when their transformers are considered: i) three-phase three-wire (3P3W) and ii) three-phase four-wire (3P4W). ΔY transformer winding connection seems to be a good arrangement option since it prevents zero sequence components from propagating to the secondary side of the transformer when an unbalanced fault occurs on the primary side network [12]. However, countries such as China and Korea [10], [12] commonly use a YY winding with neutrals grounded, see Fig. 1. In this case,

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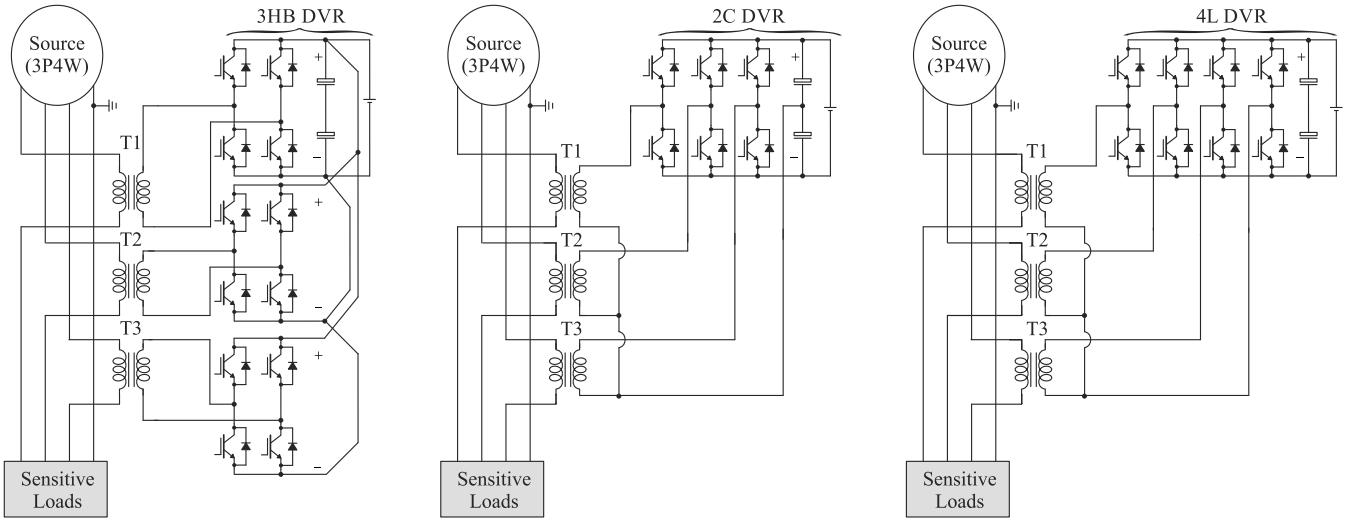

Fig. 2. Existing DVR configurations in 3P4W distribution system using injection transformers. (a) Conventional three H-Bridge (3HB) [10]. (b) Split-capacitor (2C) [12]. (c) Four-leg (4L) [13].

propagation of zero sequence components to the loads are allowed when an unbalanced fault takes place [14]. The zero sequence components propagation problem has been solved with some existing DVR topologies, see Fig. 2.

DVR technology has became a mature power quality product. Many advances have been documented in technical literature considering different aspects [8], [15]–[27]. For instance, the integration of photovoltaic and DVR systems has been proposed and validated experimentally via nine-switch converter topology in [16]. The authors in [18] focused on proposing a new phase-locked loop (named soft-PLL) and voltage sag detection algorithm based on least error square (LES) and symmetrical components method to improve the DVR performance. It was shown that the traditional algorithm achieved the steady state operation after 11 ms, while 3 ms was obtained with the proposed algorithm in [18]. The converter topology considered in that work was a cascaded H-Bridge inverter. Major studies have been validated with an experimental test rated at 10 kV [7], [17], [18], [25]. The saturation from injection transformers is another issue considered in the DVR researches. Hence, a method to avoid the saturation of transformers was proposed in [19].

It can be seen that each converter topology considered in these studies have benefits and drawbacks. So the topology selection becomes a particular design criteria to be chosen. Generally, the design criteria lies on: i) low harmonic distortion, ii) low electromagnetic interference and iii) high-voltage operation capability that is accomplished by using series connected switches. Hence, DVRs associated with a multilevel based inverter can be used to achieve most of those desirable features. In this way, a four-leg neutral point clamped (4LNPC) [28] inverter has been investigated with an optimized PWM technique. Similar results were obtained by means of a space vector PWM algorithm applied in a cascaded H-bridge (CHB) [29]. Multilevel equivalent results can be achieved by considering the concept of open-end winding (OEW) at the injection transformers of DVRs. The OEW concept is widely used in 3P3W motor drive systems [30] and recently on DVR for 3P3W systems [31].

This work investigates three options for a DVR topology on 3P4W systems application (see Fig. 3) based on the concept of OEW. Configuration 4L4L, is based on two four-leg (4L) inverters connected to injection transformers (see Fig. 3(a)). Configuration 4L2C (see Fig. 3(b)) consists of a four-leg (4L) inverter connected at one side (i.e., converter A) and split capacitor (2C) at the other side (i.e., converter B). The third one, configuration 2C2C (see Fig. 3(c)) is composed of two split capacitor (2C) configurations connected to an injection transformer in an OEW arrangement. They use more power switches than conventional ones, but enables the converter to operate with: i) lower dc-link voltage rating which reduces the switch blocking voltages and ii) lower harmonic distortion at the injected voltages by the DVR due to operation with asymmetrical dc-link voltage. Such features are the main benefits of the proposed configurations. Control system, including the PWM technique, is presented and comparisons between proposed and conventional configurations are performed. Simulation and experimental results are provided for validation purposes.

II. Models of the proposed DVR systems

The proposed DVR configurations for 3P4W systems are described in Fig. 3. All of them are based on the concept of OEW. In order to improve the paper readability, the equivalent circuit of configuration 4L4L is presented in Fig. 4(a). The modified model shown in Fig. 4(b) permits to clearly introduce the resultant output converter voltages (v_{rk}) associated for this

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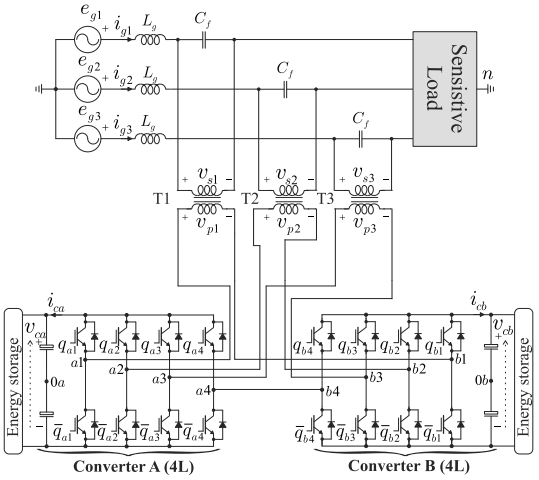
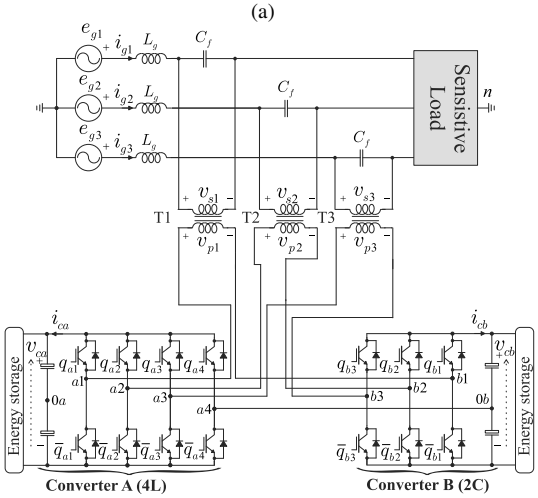
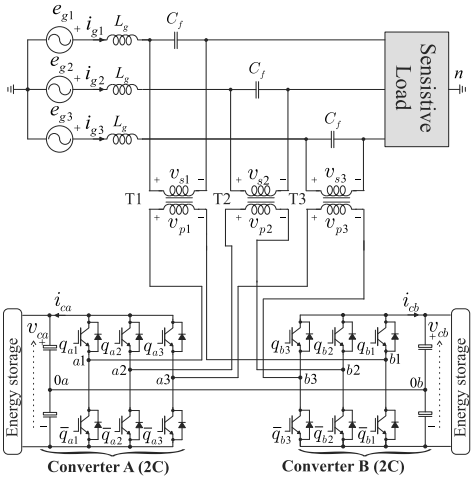


(a)



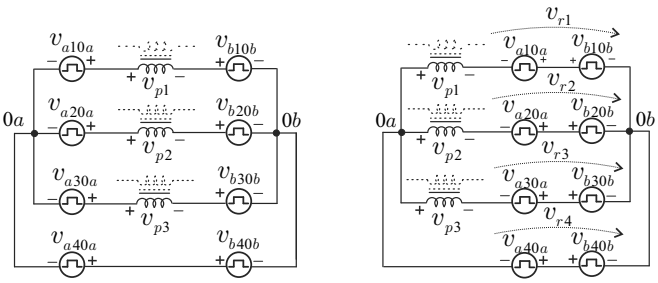
(b)



(c)

Fig. 3. Proposed OEW based DVR configurations. (a) 4L4L. (b) 4L2C and (c) 2C2C.

configuration. The model for the other configurations (i.e., 4L2C and 2C2C) is achieved by particular considerations of voltage v_{r4} (i.e., $v_{r4} = v_{a40a}$ for 4L2C and $v_{r4} = 0$ for 2C2C).



(a) (b)

Fig. 4. Equivalent circuit for configuration 4L4L. (a) Original. (b) Modified.

The pole voltages of each configuration are given by v_{ak0a} (for converter A) and v_{bk0b} (for converter B) with $k = 1, 2, 3, 4$. Such pole voltages depend on the conduction states of the power switches. The conduction state of all switches can be represented by the homonymous binary variable (e.g., for converter A $q_{ak} = 1$ indicates a closed switch while $q_{ak} = 0$ indicates an open one). Then, the pole voltages v_{ak0a} and v_{bk0b} are defined, as follows

$$v_{ak0a} = 0.5v_{ca}(2q_{ak} - 1) \quad (1)$$

$$v_{bk0b} = 0.5v_{cb}(2q_{bk} - 1) \quad (2)$$

A. Configuration 4L4L

From Figs. 3(c) and 4(a), the voltage model of configuration 4L4L is obtained as

$$v_{pj} = v_{rj} - v_{r4} \quad (3)$$

where variable $j = 1, 2, 3$ and

$$v_{rj} = v_{aj0a} - v_{bj0b} \quad (4)$$

$$v_{r4} = v_{a40a} - v_{b40b} \quad (5)$$

Note that v_{r4} is the voltage between the midpoints $0a$ and $0b$, see Fig. 4(b). Along the text $k = 1, 2, 3, 4$ and $j = 1, 2, 3$.

B. Configuration 4L2C

In this configuration, the voltage v_{pj} remains the same as in (3). However, it should be noted that $v_{r4} = v_{a40a}$ since $v_{b40b} = 0$ which is connected to the middle point of the dc-link.

C. Configuration 2C2C

This configuration has a similar model compared to conventional 3HB with regard to operation with different dc-link values. The voltages v_{pj} remain as that in (3) with $v_{r4} = 0$.

III. PWM STRATEGY

In this section, only configuration 4L4L is described in details because the PWM strategy for the other ones (4L2C and 2C2C) are obtained by particular considerations involving the reference pole voltages of the fourth leg, as discussed next.

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A. Configuration 4L4L

It can be seen from Figs. 3(a) and 4(a) that it will be necessary to calculate eight reference pole voltages (i.e., v^*_{ak0a} and v^*_{bk0b} with $k = 1, 2, 3, 4$) from three reference voltages (v^*_{p1}, v^*_{p2} and v^*_{p3}) defined from the controllers. Hence, from the degrees of freedom that system offers, five auxiliary variables are introduced, named v^*_{r4}, v^*_{x1}, v^*_{x2}, v^*_{x3}, v^*_{x4}, to determine v^*_{ak0a} and v^*_{bk0b}.

From (3)-(5) we introduce the reference voltages v^*_{rj} and v^*_{r4} (v^*_{r4} is one of the auxiliary variables) as follows

$$v^*_{rj} = v^*_{aj0a} - v^*_{bj0b} = v^*_{pj} + v^*_{r4} \tag{6}$$

$$v^*_{r4} = v^*_{a40a} - v^*_{b40b} \tag{7}$$

Introducing the last four auxiliary variables v^*_{x1}, v^*_{x2}, v^*_{x3}, v^*_{x4}, the reference pole voltages are written as follows

$$v^*_{ak0a} = \frac{1}{2}v^*_{rk} + v^*_{xk} \tag{8}$$

$$v^*_{bk0b} = -\frac{1}{2}v^*_{rk} + v^*_{xk} \tag{9}$$

To calculate the reference pole voltages v^*_{ak0a} and v^*_{bk0b}, it is necessary to calculate first the auxiliary variables v^*_{r4}, v^*_{x1}, v^*_{x2}, v^*_{x3}, v^*_{x4}. However, the limits of the pole voltages ($\pm v^*_{ca}/2$ and $\pm v^*_{cb}/2$ for the converters A and B, respectively) must be respected. The normalized choice of the auxiliary variable voltages satisfying their limits, can be provided by introducing a parameter μ ($0 \leqslant \mu \leqslant 1$) for each one (e.g., $v^*_{r4} \rightarrow \mu^*_{r4}$, $v^*_{x1} \rightarrow \mu^*_{x1}$, $v^*_{x2} \rightarrow \mu^*_{x2}$, $v^*_{x3} \rightarrow \mu^*_{x3}$ and $v^*_{x4} \rightarrow \mu^*_{x4}$).

Given v^*_{pj} from (6) and (7), the voltage v^*_{r4} is first determined according with the following expressions

$$v^*_{r4} = \mu^*_{r4}v^*_{r4\,\max} + (1 - \mu^*_{r4})v^*_{r4\,\min} \tag{10}$$

with

$$v^*_{r4\,\min} = -v^*_{cab} - \min\{v^*_{p1}, v^*_{p2}, v^*_{p3}, 0\} \tag{11}$$

$$v^*_{r4\,\max} = v^*_{cab} - \max\{v^*_{p1}, v^*_{p2}, v^*_{p3}, 0\} \tag{12}$$

where $v^*_{cab} = (v^*_{ca} + v^*_{cb})/2$ is the average dc-link capacitor reference voltage.

Once v^*_{r4} is calculated, the reference voltages v^*_{rj} are calculated from (6) and consequently all v^*_{rk} are determined. From (8) and (9) the reference voltages v^*_{xk} are calculated as

$$v^*_{xk} = \mu^*_{xk}v^*_{xk\,\max} + (1 - \mu^*_{xk})v^*_{xk\,\min} \tag{13}$$

with

$$v^*_{xk\,\min} = max\{v^*_{xak\,\min}, v^*_{xbk\,\min}\} \tag{14}$$

$$v^*_{xk\,\max} = min\{v^*_{xak\,\max}, v^*_{xbk\,\max}\} \tag{15}$$

where

$$v^*_{xak\,\min} = -v^*_{ca}/2 - v^*_{rk}/2 \tag{16}$$

$$v^*_{xbk\,\min} = -v^*_{cb}/2 + v^*_{rk}/2 \tag{17}$$

$$v^*_{xak\,\max} = v^*_{ca}/2 - v^*_{rk}/2 \tag{18}$$

$$v^*_{xbk\,\max} = v^*_{cb}/2 + v^*_{rk}/2 \tag{19}$$

The following algorithm summarizes the PWM strategy applied for configuration 4L4L.

Step 1: Determine v^*_{r4}.

a) Given v^*_{pj}, determine $v^*_{r4\,\min}$ and $v^*_{r4\,\max}$ using relations (11) and (12), respectively;

b) Choose μ^*_{r4} and determine v^*_{r4} using (10);

Step 2: Determine v^*_{rj} from (6).

Step 3: Determine v^*_{xk}.

a) From v^*_{rk}, determine $v^*_{xk\,\min}$ and $v^*_{xk\,\max}$ using relations (14) and (15), respectively;

b) Choose μ^*_{xk} and determine v^*_{xk} using (13);

Step 4: Determine v^*_{ak0a} and v^*_{bk0b} using relations (8) and (9), respectively.

The modified model obtained by considering voltages v^*_{rk} (i.e., v^*_{rj} and v^*_{r4}) is observed in Fig. 4(b). It indicates that once calculated v^*_{rk} from steps 1 and 2, the steps 3 and 4 correspond to apply a PWM strategy to solve the pole voltages for four H-bridge inverters.

B. Configuration 4L2C

In this configuration, there are only four auxiliary variables (v^*_{r4}, v^*_{x1}, v^*_{x2} and v^*_{x3}). The reference pole voltage v^*_{a40a} is equal to v^*_{r4}. In this case, $v^*_{r4\,\min}$ and $v^*_{r4\,\max}$ are given by

$$v^*_{r4\,\min} = \max\{v'^*_{r4\,\min}, v''^*_{r4\,\min}\}$$

$$v^*_{r4\,\max} = \min\{v'^*_{r4\,\max}, v''^*_{r4\,\max}\}$$

where

$$v'^*_{r4\,\min} = -v^*_{cab} - \min\{v^*_{p1}, v^*_{p2}, v^*_{p3}\}$$

$$v'^*_{r4\,\max} = v^*_{cab} - \max\{v^*_{p1}, v^*_{p2}, v^*_{p3}\}$$

$$v''^*_{r4\,\min} = -v^*_{ca}/2$$

$$v''^*_{r4\,\max} = v^*_{ca}/2$$

After steps 1 and 2, steps 3 and 4 solve the pole voltages for three full H-bridges and one half H-bridge.

C. Configuration 2C2C

For this configuration, there are six pole voltages. Hence, the PWM strategy have only three auxiliary variable voltages (v^*_{x1}, v^*_{x2}, v^*_{x3}), since $v^*_{r4} = 0$. Consequently, step 1 is not necessary and after step 2 (i.e., $v^*_{rj} = v^*_{pj}$), steps 3 and 4 determine the pole voltages for three full H-bridges.

D. Choice of the parameters μ^*_{r4} and μ^*_{xk}

In all three configurations, the reference pole voltages are compared with carrier signals in order to obtain the state of the power switches. The values of parameters μ^*_{r4} and μ^*_{xk} are chosen in order to reduce the harmonic distortion of the voltage generated by the converters A and B. The determination of parameters μ^*_{xk} and the carriers disposition to solve the pole voltages calculation of equivalent H-bridge was done with a similar approach presented in [31].

Another alternative way for choosing parameters μ^*_{r4} and μ^*_{xk} is to consider their values in order to share the power processed between the dc links of converters A and B. This option permits to minimize the active power in one dc-link. In this way, such a dc-link could be considered as a very low energy storage source (e.g., a battery with low voltage rating) or even as a floating dc-link capacitor for fault tolerance capability.

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IV. SYSTEM CONTROL

In DVR applications, open loop and closed loop are control methods well accepted and used in the literature [32]–[34]. In this paper, an open loop load voltage control, combined with feed forward compensation that deals with voltage drop caused by filter C_f, was considered. In this way, grid voltages (e_{gj}) are measured and compared with rated load voltages (v^*_{lj}). The comparison result gives the references to the injected voltages ($v^*_{pj} = e_{gj} - v^*_{lj}$). A feed forward action can be used in order the compensated voltage drop (v_{cf}) in the passive filters. Hence, the references become $v^*_{pj} = e_{gj} - v^*_{lj} + v_{cf}$. The voltage sag detection scheme used in this paper is similar to that one used in [34]. The reference voltages v^*_{pj} must be synchronized with e_{gj}. In this way, a phase-locked loop based on fictitious electrical power (i.e., power-based PLL) [35] was considered.

V. TOPOLOGICAL COMPARISON

The minimum dc-link voltage required (i.e., v^*_{cab} for proposed or v^*_c for conventional) for each dc-link of the topologies investigated in this work was compared. This specification reflects on the peak inverse voltages (PIV) at each power switch. It can be seen also the number of semiconductor devices and capacitors needed for each topology. In this comparison two cases are considered with maximum balanced voltages in dq-frame: i) without zero sequence voltage (v_0) and ii) with zero sequence voltage injection (v_0).

Table I presents a dc-link voltage comparison in which the converter produces a maximum balanced voltages with no zero sequence voltage. In this way, the three-phase voltages v_{pj} (i.e., v_{p1}, v_{p2} and v_{p3}) are symmetrical and balanced as follows

$$v_{pj} = V_{pdq} sin(wt - 2(j-1)\pi/3) \tag{20}$$

where V_{pdq} is the maximum voltage amplitude in dq-frame available at the primary side of the injection transformers and $w = 2\pi f_o$ in which f_o is the fundamental system frequency.

Then, considering the parameter v^*_{cab}, configurations 4L4L and 4L2C have presented a reduction of 56% in comparison with 2C topology. In comparison with the topology 4L, the configurations 4L4L and 4L2C can be reduced up to 50%. Lastly, the voltage v^*_{cab} for both of them (i.e., 4L4L and 4L2C) can be reduced up to 15% compared to conventional 3HB and proposed 2C2C. Nevertheless, they have a higher number of IGBTs as well as capacitors. The proposed 2C2C topology provides the same dc-link voltage rating if compared to 3HB one but it takes advantage of its different dc-link voltages operation capability. Hence, such a topology (2C2C) can generate the voltages v_{pj} with lower harmonic distortion in comparison with 3HB topology.

Taking into consideration conventional multilevel structures, similar comparison can be observed with a conventional four-leg neutral-point-clamped (4LNPC) configuration [28]. It can be seen that 4LNPC presents the same power switches count (i.e., 16 IGBTs) and dc-link capacitors (i.e., 2 capacitors) as for 4L4L. However, 4LNPC needs 8 additional clamping diodes that are not needed for any one of proposed configurations.

TABLE I
TOPOLOGICAL COMPARISON. v^*_{cab} IS FOR PROPOSED CONFIGURATIONS AND v^*_c IS FOR CONVENTIONALS.

Topology	v^*_{cab} or v^*_c	IGBTs	Capacitors
Conventional 2C	$2.00V_{pdq}$	6	2
Conventional 3HB	$1.00V_{pdq}$	12	1
Conventional 4L	$1.73V_{pdq}$	8	1
Conventional 4LNPC	$1.73V_{pdq}$	16	2
Proposed 4L4L	$0.87V_{pdq}$	16	2
Proposed 2C2C	$1.00V_{pdq}$	12	4
Proposed 4L2C	$0.83V_{pdq}$	14	3

For the case in which v_{pj} have zero sequence voltage (v_0), the configurations 4L4L, 4L and 4L2C can generate a parcel of that voltage with the same dc-link value shown in Table I (obtained without zero sequence voltage). Hence, it can be written

$$v_{pj} = V_{pdq} sin(wt - 2(j-1)\pi/3) + V_{po} sin(wt) \tag{21}$$

where V_{po} is the maximum amplitude of the zero sequence voltage.

The maximum amplitude of V_{po} that can be achieved for each configuration is given by

- 4L4L and 4L:

$$V_{po} \leq 0.732 V_{pdq} \tag{22}$$

- 4L2C:

$$V_{po} \leq 0.2990 V_{pdq};\ \text{if } v_{ca} = v_{cb} \tag{23}$$

$$V_{po} \leq 0.1547 V_{pdq};\ \text{if } v_{ca} = v_{cb}/2 \tag{24}$$

$$V_{po} \leq 0.4434 V_{pdq};\ \text{if } v_{ca} = 2v_{cb} \tag{25}$$

VI. COMPARISON OF SWITCHING VECTORS AVAILABLE

There are 16 (2^4) and 64 (2^6) switching states in the case of conventional 4L and 3HB based DVR, respectively. For 4L and 3HB configurations, those switching states generate 15 and 27 different switching vectors, respectively. Fig. 5 shows all vectors available for these conventional configurations in 3D (dqo space). Notice that 2C2C configuration with dc-link ratio 1:1 (that means $v_{ca} = v_{cb}$) is equivalent to 3HB one.

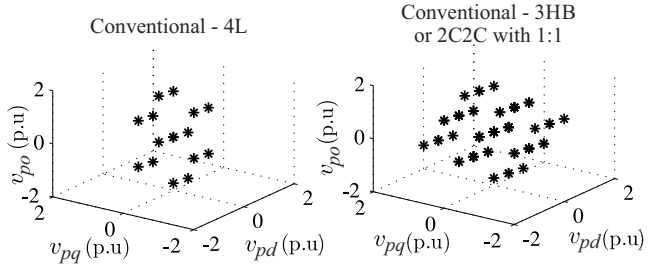

Fig. 5. Output voltage space and the switching vectors available for conventional inverters. Conventional 4L (on the left). Conventional 3HB or 2C2C with dc-link ratio 1:1 (on the right).

Fig. 6 shows the switching vectors available for the proposed 2C2C configuration considering two cases of dc-link

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values: i) case 1:2 (that means $v_{ca} = 2v_{cb}$) and ii) case 1:3 (meaning $v_{ca} = 3v_{cb}$), both of them generating 64 different switching vectors. However, case 1:3 presents a more asymmetrical switching vectors distribution if compared to the case 1:2. Comparing with 3HB, proposed 2C2C with dc-link ratios of either 1:2 or 1:3 has also 64 switching states but it provides more different switching vectors (i.e., 64 instead of 27 obtained with 3HB).

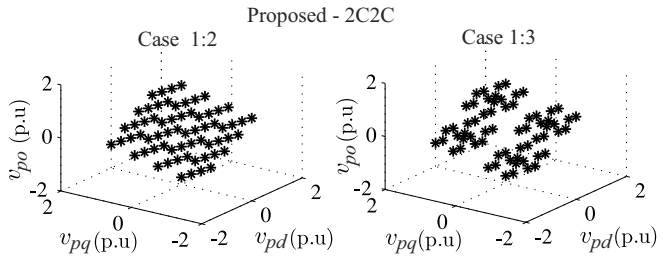

Fig. 6. Output voltage space and the switching vectors available for proposed 2C2C. Operation with dc-link ratio 1:2 (on the left). Operation with dc-link ratio 1:3 (on the right).

The proposed 4L2C configuration has 128 (2^7) switching states. Then, as expected, the number of different vectors increases in comparison with the previous one, as observed in Fig. 7. In this result, case 1:1 ($v_{ca} = v_{cb}$) presents 46 different switching vectors whereas case 1:2 ($v_{ca} = 2v_{cb}$) has 101 different switching vectors. The case 1:3 for this configuration is not shown due to its more asymmetrical switching vectors distribution than that one obtained for case 1:2. Such a sort of deterioration is already shown in Fig. 6 for configuration 2C2C.

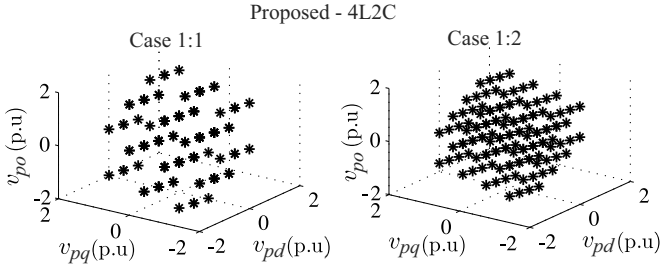

Fig. 7. Output voltage space and the switching vectors available for proposed 4L2C configuration. Operation with dc-link ratio 1:1 (on the left). Operation with dc-link ratio 1:2 (on the right).

Fig. 8 shows a similar result for configuration 4L4L. Such a result shows that 65 different switching vectors are obtained in case 1:1 whereas 175 different switching vectors are obtained in case 1:2.

Comparing with the 2C2C and the conventional ones, it can be seen that both 4L2C and 4L4L provide high number of different switching vectors. However, some of them have high values of v_{po} component that maybe will not be used if the inverters operate with low v_{po} magnitude.

VII. HARMONIC DISTORTION

The weighted total harmonic distortion (WTHD) of the injected voltages (v_{pj}) for conventional 3HB and proposed configurations have been computed by using

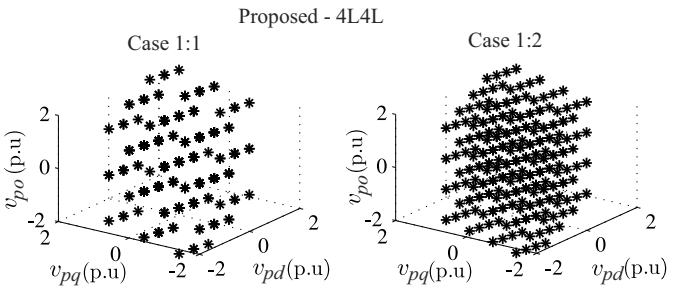

Fig. 8. Output voltage space and the switching vectors available for proposed 4L4L configuration with dc-link ratios 1:1 (on the left) and 1:2 ratio (on the right).

$$WTHD(p) = \frac{100}{a_1}\sqrt{\sum_{i=2}^{p}\left(\frac{a_i}{i}\right)^2} \tag{26}$$

where a_1 is the amplitude of the fundamental voltage, a_i is the amplitude of i^{th} harmonic and p is the number of harmonics taken into consideration. Then, by imposing the same operation conditions that are a maximum injection of v_{pj} in a balanced three-phase case, WTHD of the injected voltages (v_{pj}) for conventional 3HB and proposed configuration can be observed in Table II. In this result, both average switching frequency (f_s) and fundamental frequency (f_o) were fixed in 10 kHz and 50 Hz, respectively.

It should be noticed that 2C2C topology operating with dc-link ratio 1:1 ($v_{ca} = v_{cb}$) is equal to conventional 3HB. Such cases permit to conclude that the best (minimum) WTHD value is achieved with proposed 4L4L. Nevertheless all proposed configurations present lower WTHD values in comparison with conventional 3HB that has best WTHD value among the conventional ones.

TABLE II
WHTD FOR CONVENTIONAL AND PROPOSED CONFIGURATIONS ($f_s = 10$ KHZ; $f_o = 50$ HZ).

Topology	Dc-link ratio	WTHD (%)
Conventional 3HB	-	0.22
Proposed 2C2C	1:2	0.14
	1:3	0.15
Proposed 4L2C	1:1	0.19
	1:2	0.12
	1:3	0.34
Proposed 4L4L	1:1	0.12
	1:2	0.11
	1:3	0.11

VIII. CONVERTER POWER LOSSES

The loss estimation was obtained through regression model, which has been achieved by experimental tests as presented in [36] and [37]. The thermal module, an existing tool in PSIM $v9.0$ was used with calibration parameters that gives an equivalent estimation. The power switch used in the experimental tests was: IGBT dual module CM50DY-24H (POWEREX) driven by SKHI-10 (SEMIKRON). The switch losses model includes: a) IGBT and diode conduction losses; b) IGBT turn-on losses;c) IGBT turn-off losses; d) Diode turn-off energy.

Fig. 9 shows a result with five cases in which the proposed DVR configuration losses have been compared with

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the conventional 3HB under the same operation conditions (i.e., four cases with maximum balanced three-phase voltages without zero sequence component and a fifth case with zero sequence component) and with the same harmonic distortion content (WTHD = 0.22%) for v_{pj}. For instance, the average switching frequency (f_s) has been fixed in 10 kHz, 6.25 kHz, 5.3 kHz and 4.8 kHz for 3HB, 2C2C, 4L2C and 4L4L, respectively. Such values guarantee that DVRs will generate the voltages v_{pj} with the same harmonic distortion. Different dc-link voltage values were considered (i.e., 1:2). The results have been normalized with conventional 3HB (total losses close to 58 W). Notice that the proposed configurations present lower switching losses and increased conduction losses on the proposed configuration as a consequence of their high number of IGBTs. Nevertheless, the total losses are lower in comparison with conventional 3HB.

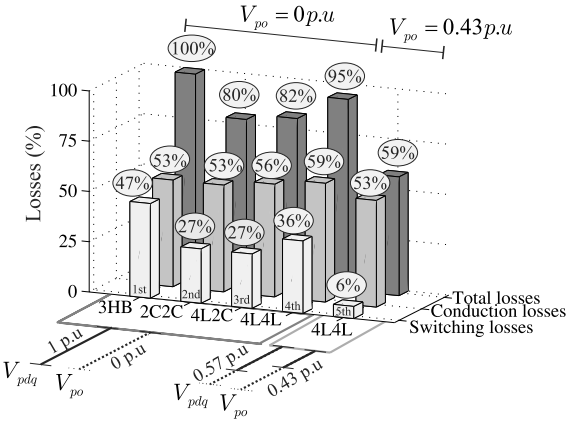

Fig. 9. Semiconductor losses comparison between conventional 3HB and proposed configurations operating with dc-link ratio 1:2 under the same harmonic distortion content at v_{pj}. First four results (from the left to right) with $V_{po} = 0$ and fifth result with 57% of V_{pdq} and 43% of V_{po}.

The fourth leg connected to the neutral will improve the performance of the system under zero-sequence voltage compensation as well as offers the possibility to control zero-sequence voltage. In this case, the fifth result of losses in Fig. 9 shows a case for configuration 4L4L in which 57% of V_{pdq} is compensated leading 43% of compensation for V_{po}. In this way, the converter can operate with dc-link voltage ($v_{ca} + v_{cb}$) equal to $\sqrt{3}V_{pdq}$ (the same value used for $V_{po} = 0$). Additionally, the voltage waveforms of v_{pj} are improved in terms of WTHD, which permits to reduce switching frequency up to 2.55 kHZ to maintain the same WTHD of v_{pj} obtained for the other cases (i.e., WTHD = 0.22%). Hence, the possibility to hand out the zero-sequence to fourth leg justifies: i) dc-link voltage reduction and ii) the waveform quality of v_{pj} that leads switching frequency reduction to operate under the same WTHD of conventional 3HB. Asymmetric dc-link voltage operation was employed in this result (i.e., dc-link voltage ratio 1:2).

IX. DC-LINK HIGH FREQUENCY POWER LOSSES

In this section, a comparative study of dc-link power losses estimation has been made. In this case, the operation of conventional and proposed configurations was fixed with the same WTHD conditions for the injected voltages (v_{pj}).

The dc-link high frequency power losses is calculated by

$$P_{loss}^{HO} = N(0.45)ESR_{(100Hz)} \left(I_{c,rms}^{HO}\right)^2 \quad (27)$$

where N is the number of capacitors used in each topology, $I_{c,rms}^{HO}$ is the component of the high-order of the root mean square (RMS) current on the dc-link (with $h > 50$) and $ESR_{(100Hz)}$ is the equivalent series resistance for a frequency of 100 Hz. The ESR can be considered constant for frequency higher than 3 kHz. It is equal to 0.45 times of ESR value for 100 Hz [38]. This means that P_{loss}^{HO} depends only of the $I_{c,rms}^{HO}$.

Fig. 10 shows harmonic spectrum of dc-link currents for comparison purposes with different dc-link voltage values (i.e., considering dc-link ratio 1:2). It can be observed that the equivalent harmonic current content for proposed OEW configurations does not exceed the magnitude of conventional 3HB one.

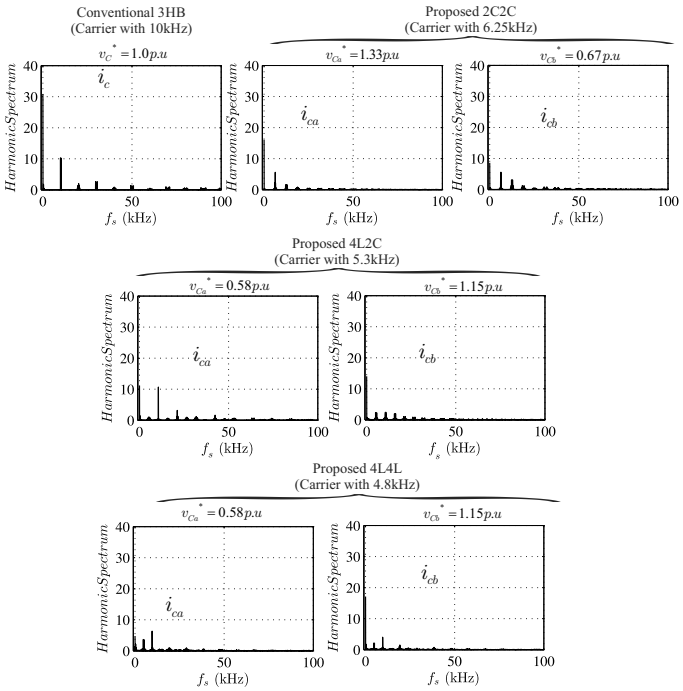

Fig. 10. Harmonic spectrum of the capacitor currents for conventional 3HB and proposed configurations.

Table III presents the dc-link high frequency power losses normalized by power losses of conventional 3HB configuration (i.e, $P_{loss}^{HO}/P_{loss(3HB)}^{HO}$). Notice that the proposed 4L4L presents a reduction of 64% in dc-link high frequency power losses compared to conventional 3HB, whereas 2C2C and 4L2C presented a reduction of 23% and 39%, respectively.

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TABLE III
LOSSES COMPARISON OF THE DC-LINK.

Normalized dc-link losses				
Topology	**3HB**	**2C2C**	**4L2C**	**4L4L**
$P_{loss}^{HO}/P_{loss(3HB)}^{HO}$	1.00	0.77	0.61	0.36

X. SIMULATION RESULTS

Conventional 3HB and proposed DVR configurations have been evaluated through simulation by using PSIM $v9.0$ and MATLAB®. The dc-link voltages were considered as auxiliary energy DC sources (i.e., isolated batteries). The simulation step (h) was fixed in 0.5 μs and the switching frequency (f_s) was considered as 10 kHz. The load type was considered as resistance bank of 100 Ω.

Fig. 11 shows the injected voltages (not filtered) by DVR considering equal ($v_{ca} = v_{cb}$) and different ($v_{ca} \neq v_{cb}$) dc-link voltage values for proposed configurations. The cases investigated in Fig. 11 show that the injected voltages by the proposed DVRs provide more levels and as a consequence they present lower WTHD in comparison with the conventional 3HB one under the same conditions of operation.

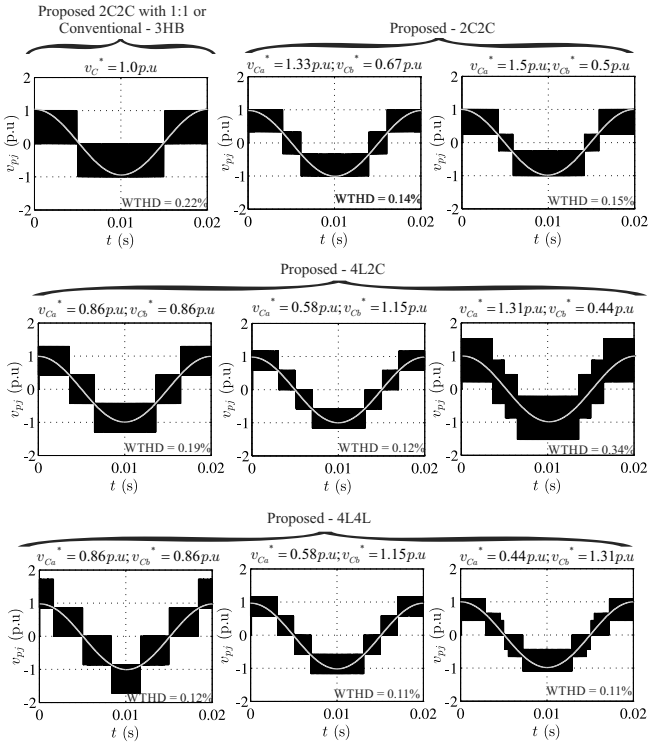

Fig. 11. Injected voltages by the DVR considering conventional 3HB topology and proposed configurations with equal dc-link voltages ($v_{ca} = v_{cb}$ → dc-link ratio 1:1) and different dc-link voltages ($v_{ca} \neq v_{cb}$ → dc-link ratios 1:2 and 1:3).

The system performance with proposed DVR 4L4L operating with equal dc-link voltages ($v_{ca} = v_{cb}$) has been investigated under: i) single-phase voltage sag (see Fig. 12), ii) two-phase voltage sag (see Fig. 13) and iii) three-phase voltage sag (see Fig. 14). The magnitude of the voltage sag was the same for three cases (i.e., 30%) with time duration close to 200 ms. It can be seen that the proposed 4L4L DVR compensated the voltage sags satisfactorily. The results for configurations 2C2C, 4L2C are similar.

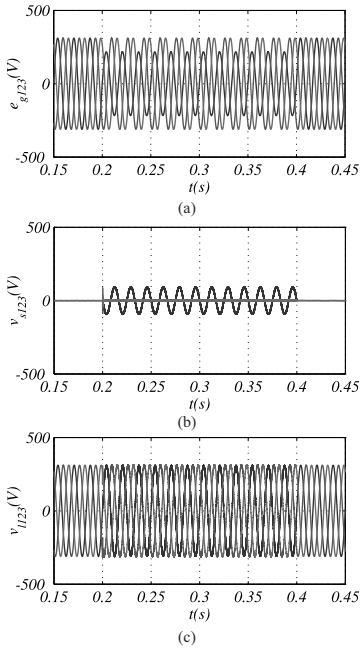

Fig. 12. System operation in time domain considering configuration 4L4L. The DVR compensates a 30% single-phase voltage sag. (a) Grid voltages. (b) Injected voltages by the DVR. (c) Load voltages.

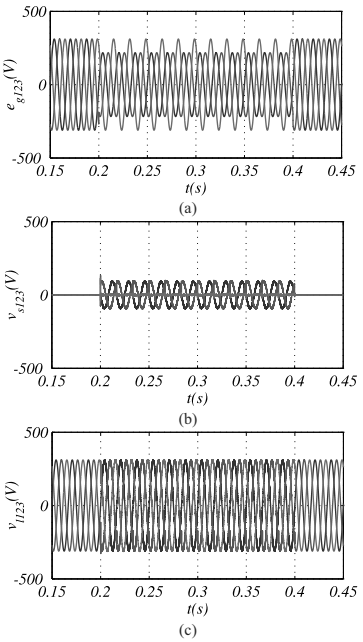

Fig. 13. System operation in time domain considering configuration 4L4L. The DVR compensates a 30% two-phase voltage sag. (a) Grid voltages. (b) Injected voltages by the DVR. (c) Load voltages.

XI. EXPERIMENTAL SYSTEM SPECIFICATIONS

The Proposed DVRs, shown in Fig. 3, have been validated in laboratory via some experimental tests. Such tests were made with a downscaled prototype system. The grid line-neutral voltage was considered as 70 V (RMS) and the

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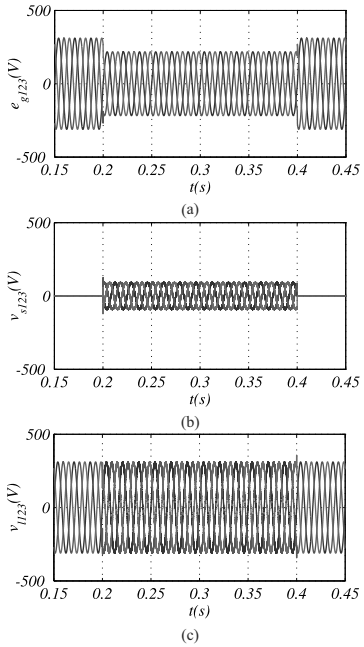

Fig. 14. System operation in time domain considering configuration 4L4L. The DVR compensates a 30% three-phase voltage sag. (a) Grid voltages. (b) Injected voltages by the DVR. (c) Load voltages.

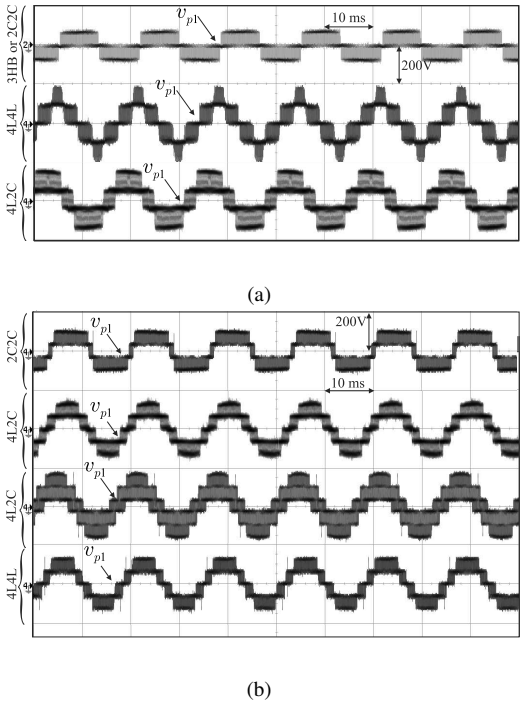

Fig. 15. Experimental results. Voltage v_{p1} for each proposed configuration and conventional 3HB (or 2C2C). (a) 3HB or 2C2C (top), 4L4L (middle) and 4L2C (bottom) operating with dc-link ratio 1:1 ($v_{ca} = v_{cb} = 100$ V). (b) 2C2C (top), 4L2C (middle 1: $v_{ca} = 67$ V and $v_{cb} = 133$ V), 4L2C (middle 2: $v_{ca} = 133$ V and $v_{cb} = 67$ V) and 4L4L (bottom) operating with dc-link ratio 1:2 ($v_{ca} = 133$ V and $v_{cb} = 67$ V).

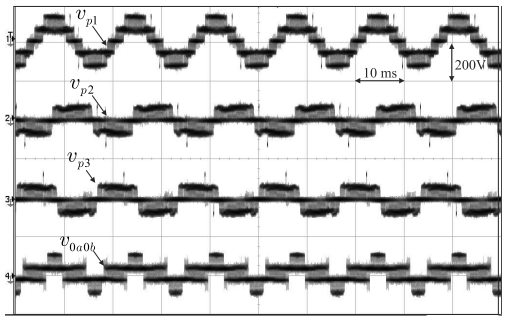

Fig. 16. Experimental results. Injected voltages by DVR with 4L4L configuration compensating 35% of zero sequence component. The inverters operate with $v_{ca} = 133$ V and $v_{cb} = 67$ V.

voltage sag generator was implemented with 50 Ω / 200 W resistors connected in series with the downscaled grid. The load type considered in the tests was a resistors bank (incandescent lamps). The dc-link voltages of the converters A and B were obtained from two rectifiers (isolated from each other) connected to ac-lines by means of an auxiliary autotransformer.

The dc-link capacitors were selected as C = 2200 μF, the switching frequency (f_s) employed was 10 kHz. The three used injection transformers have a power rated equal to 1 kVA each, with turn ratios from the primary to the secondary winding equal to 1:1. The core of the transformers is made of ferromagnetic grain-oriented material in a toroidal shape. Such a characteristic minimizes their leakage inductance. Three capacitors C_f were connected at the secondary winding of each injection transformer in order to filter high order harmonics provided from the PWM converters. The filtering capacitors were selected as C_f = 30 μF.

The converters used for the prototype are composed of IGBTs power switches from semikron (SKM50GB123D) driven by SKHI23, which receives gating signals throughout optical fiber cables linked to a digital signal processor (DSP) TMS320F28335 with a microcomputer equipped with appropriated plug-in boards and sensors.

XII. EXPERIMENTAL RESULTS

Experimental results presented in Fig. 15 show the PWM validation for the proposed DVRs. The phase-voltage at the primary side of the transformer (v_{p1}) is presented for one phase for each configuration. Fig. 15(a) shows the operation with $v_{Ca} = v_{Cb}$ (i.e., dc-link ratio 1:1) whereas the cases of different dc-link voltages (i.e., dc-link ratio 1:2) are shown in Fig. 15(b). It can be observed that these outcomes are similar to simulation results presented previously in Fig. 11.

Fig. 16 shows results in which the configuration 4L4L processes 50% of dq voltage component and 35% of zero sequence component. In this way, the references are

$$v_{pj} = 0.5V_{pdq}sin(wt - 2(j-1)\pi/3) + V_{po}sin(wt) \quad (28)$$

with $V_{pdq} = 2v^*_{cab}/\sqrt{3}$ and $V_{po} = 0.35V_{pdq}$.

The dynamic operation of the proposed DVRs has been tested experimentally. Fig. 17 shows results in which the DVRs compensate an unbalanced 35% three-phase voltage sag with time duration close to 400 ms. It can be seen that the load voltages are well compensated. The time interval between the voltage sag occurrence and the DVR action was close to 4 ms for the three configurations. The voltage transients (spikes)

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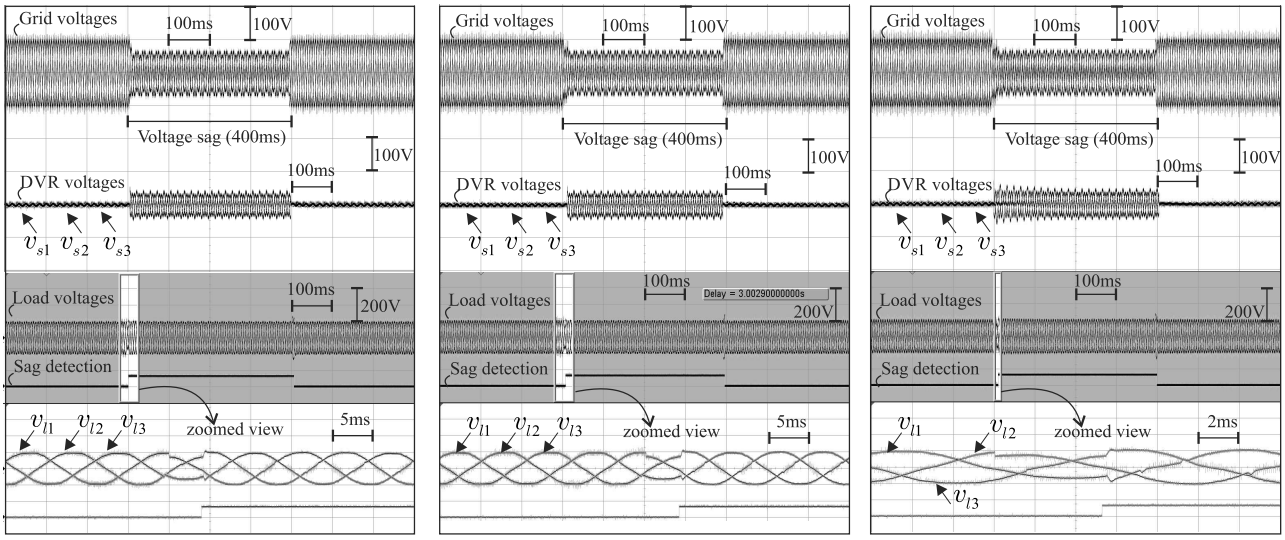

Fig. 17. Experimental results. System voltages considering three proposed DVR configurations operating with asymmetric dc-link voltages under an unbalanced 35% three-phase voltage sag with 400 ms duration. (a) Proposed 4L4L. (b) Proposed 4L2C. (c) Proposed 2C2C.

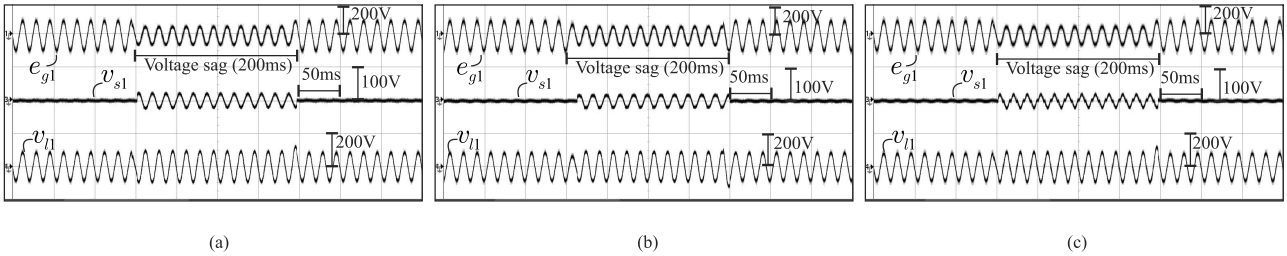

Fig. 18. Experimental results. System voltages at phase 1 considering three proposed DVR configurations operating with asymmetric dc-link voltages under 40% single-phase voltage sag with 200 ms duration. (a) Proposed 4L4L. (b) Proposed 4L2C. (c) Proposed 2C2C.

observed on the load voltages both at the start or return transition of voltage sag are due to the filtering capacitors (C_f). This phenomena was observed also in some studies in the literature and can be attenuated with a more accurate control method or by using a robust passive filter (e.g., LCL filter type) as discussed in [32], [34].

Fig. 18 shows the DVR compensation under a 40% single-phase voltage sag generated at the grid voltage (e_{g1}) during 200 ms, with proposed configurations operating with different dc-link voltages. In this way, once the voltage sag is detected the converters start to operate by applying voltage directly at the primary side of injection transformer. This voltage is filtered by filtering capacitors C_f giving the necessary voltage v_{s1} to be compensated by the DVR. Outcomes are shown only for the disturbed phase (i.e., phase 1). It can be seen that the load voltage (v_{l1}) keeps its magnitude fixed at 1 p.u that means a satisfactory compensation. Fig. 18(a) shows results for 4L4L configuration operating with $v_{ca} = 2v_{cb}$. The same scenario considering topology 4L2C is shown in Fig. 18(b) in which the dc-link voltage ratio is $v_{ca} = 0.5v_{cb}$. The result is shown similarly for configuration 2C2C in Fig. 18(c) with $v_{ca} = 2v_{cb}$.

XIII. CONCLUSION

In this paper, three four-wire dynamic voltage restorers (DVRs) have been proposed. The studied configurations are based on the concept of open-end winding. Compared to conventional 3HB, the proposed ones have presented advantages in terms of lower WTHD, semiconductor losses, dc-link high frequency losses and low dc-link voltage rating. On the other hand, 4L4L and 4L2C topologies have an increased switch count. It is noted that the dc-link voltage reduction is more evident for configurations 4L4L and 4L2C with the increasing of the zero sequence voltage magnitude (V_{po}). This is because the zero sequence parcel can only be fully controlled by the fourth legs of each converter (i.e., 2 legs for 4L4L and 1 leg for 4L2C). For configuration 3HB and 2C2C this flexibility is lost because the zero-sequence voltage will be controlled over the six legs connected to the wires 1, 2 and 3 of the DVR. However, the maximum value achieved by V_{po} will be different accordingly to each configuration, as discussed in Section V.

The outcomes have shown that proposed DVRs are feasible and suitable for three-phase four-wire (3P4W) power distribution systems in which low harmonic distortion is a priority since it leads to reduce the switching frequency to match the same WTHD value that is obtained with conventional configuration. However, notice that conventional one will operate with higher frequency rating. The proposed configurations have advantages in high-voltage systems that would be unlikely to be achieved with some conventional configurations (e.g., 2C and 4L configurations).

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